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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,995	09/27/2001	Kazuo Ogawa	N29748500S	2991

7590 04/26/2002

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EXAMINER
TRAN, THIEN F

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,995	OGAWA, KAZUO	
	Examiner	Art Unit	
	Thien F Tran	2811	

-- The MAILING DATE of this communication app ars on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-11 in Paper No. 6 is acknowledged.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

Claim 1 is objected to because of the following informalities: line 8, "a top section of the trench" should be --inner wall edges in a top section of the trench--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-9 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishitsuka et al. (US 6,242,323).

Ishitsuka et al. discloses the claimed semiconductor device (Fig. 32) comprising a trench element separation region 4 including a trench 4a formed in a surface of a semiconductor substrate, the trench element separation region isolating separate semiconductor elements (isolating a first doped channel layer 14 of a first insulated gate field effect transistor from a second doped channel layer 15 of a second IGFET); an oxide film 5 formed on inner walls of the trench; a trench filling insulating material 7 filling the trench and having (vertical) edges above the inner walls of the trench; and wherein inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same vertical plane.

Regarding claims 2 and 8, the vertical edges of the trench filling insulating material are defined by side edges of a sacrificial layer 3.

Regarding claim 3, the sacrificial layer is a silicon nitride film.

Regarding claim 5, the semiconductors elements are insulated gate field effect transistors (IGFETs).

Regarding claim 6, the IGFETs include opposite conductivity types.

Regarding claim 11, the first and second doped channel layers (14, 15) are of opposite conductivity types.

Regarding claims 4 and 9, the claim limitation "formed by an etching process including a neutral radical" in claim 4, and "formed by an etching process including a fluorine radical" in claim 9 are taken to be product by process limitations. A product by process claim directed to the product per se, no matter how actually made, In re Hirao,

190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Claim 7 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Bhakta et al. (US 6,258,697).

Bhakta et al. discloses the claimed semiconductor device (Fig. 3G) comprising a trench element separation region including a trench 40 formed in a surface of a semiconductor substrate, the trench element separation region isolating a first doped channel layer 49 of a first insulated gate field effect transistor from a second doped channel layer 49 of a second IGFET; an oxide film 42 formed on inner walls of the trench; a trench filling insulating material 46 filling the trench and having edges above the inner walls of the trench; and wherein inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane.

Regarding claim 10, the first and second doped channel layers 49 are doped at the same time. It is inherent that the first and second doped channel layers 49 are doped of the same conductivity type.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 7:00AM - 3:30PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt
April 16, 2002

Thien Tran
Patent Examiner
Technology Center 2800